Abstract:
For the wireless communication in radio frequency range, IEEE 802.11 is one of the many standards available. IEEE 802.11b defines the Medium Access Control Layer [MAC] for wireless local area networks. The wireless local area network, WLAN is dominated by IEEE 802.11 standard. It becomes one of the main focuses of the WLAN research. Now most of the ongoing research projects are simulation based as their actual hardware implementation is not cost effective.

The main core of the IEEE 802.11b standard are the CSMA/CA, Physical and MAC layers. But only MAC layer for transmitter is modeled in this paper using the VHDL. The VHDL (Very High Speed Hardware Description Language) is defined in IEEE as a tool of creation of electronics system because it supports the development, verification, synthesis and testing of hardware design, the communication of hardware design data and the maintenance, modification and procurement of hardware. It is a common language for electronics design and development prototyping.

The main purpose of the IEEE 802.11 standard is to provide wireless connectivity to devices that require a faster installation, such as Laptops, PDA's or generally mobile devices inside a WLAN. MAC procedures are defined here for accessing the physical medium, which can be infrared or radio frequency.

Here Wi-Fi MAC Transmitter module is divided in to 5 blocks i.e. Data Unit Interface block, Controller block, Payload Data Storage block, MAC Header Register block, Data Processing block. In this paper, we are considering only two blocks i.e. Payload Data Storage block & Data Processing block. So, other blocks i.e. Data Unit Interface block, Controller block, MAC Header Register block are not discussed further in this paper.

Keywords: WLAN, IEEE 802.11, VHDL, Wi-Fi MAC layer, FPGA

1. Introduction to IEEE 802.11

Due to technology advancement in the 21st Century, wireless Communication had been most popular choices of communication. More and more people are turning to wireless due to the convenience of mobility. An 802.11 LAN is based on a cellular architecture where the system is subdivided in to cells, where each cell [called Basic Service Set or BSS] is controlled by a Base Station [called Access point, or in short AP]. Even though that a wireless LAN may be formed by a single cell, with a Single Access Point can also work without an Access Point, most installations will be formed by several cells, where the Access Points are connected through some kind of back bone [called Distribution System or DS], typically Ethernet, and in some cases wireless it self. The whole interconnected wireless LAN including the different cells, their respective Access Points and the Distribution System, is seen to the upper layers of the OSI model, as a single 802 network and is called in the standard as Extended Service Set[ESS]. The standard also defines the concept of a portal, a portal is a device that interconnects an 802.11 and another 802 LAN [3].

However, all is not predestined in the WLAN world. Offering nominal bit rates of 11Mbps [802.11b] and 54Mbps [802.11a and 802.11g] the effective throughputs are actually much lower owing to packet collisions, protocol overhead, and interference in the increasingly congested unlicensed bands at 2.4GHz and 5GHz. Further more, operation in these bands entails a strict regulatory transmit power constraint, thus limiting range and even bit rates beyond a certain distance [5].

2. Overview of MAC layer:

The 802.11 protocol covers the MAC and physical layer, the standard currently defines a single MAC which interacts with three physical layers [all of them running at 1 and 2 Mbits/sec] i.e. Frequency Hopping Spread Spectrum in the 2.4GHz band, Direct Sequence Spread Spectrum in the 2.4GHz band and Infrared[3]. Beyond the standard functionality usually performed by MAC layers, the 802.11 MAC performs other functions that are typically related to upper layer protocols, such as Fragmentation, Packet retransmissions and Acknowledgements. The MAC layer defines two access methods, the Distribution Coordination Function [DCF] and Point Coordination Function [PCF][3].

MAC layer acts as an intermediate stage between Data Link Layer and Physical Layer. It’s primary responsibility is to provide a reliable mechanism for exchanging transmitting packets [Data, Control and Management] on the communication channel through physical layer [RF layer]. MAC layer performs the following transmit functions i) Generation of various MAC frames [Data, Control, and Management] ii) Generation of 16 bit HEC for Header and 32 bit CRC for payload data iii) CRC and HEC generation for payload & Header respectively iv) FIFO buffer interface for transmitter v) Serializing the data using byte to bit converter vi) MAC transmitter controller state machine implementation.
Medium Access control [MAC] layer performs function like i) On transmission, assemble data in to a frame with address and error detection fields ii) On reception, disassemble frame and perform address recognition and error detection iii)Govern access to the LAN transmission medium. Physical layer performs functions like. i) Encoding/decoding of signals ii) Preamble generation/ removal [for Synchronization]. iii) Bit transmission / reception iv) Includes specifications of the transmission medium [4].

3. Wi-Fi features:

Wi-Fi Wireless Fidelity [802.11 family of standards] for LAN. WiFi is designed for local area networks, which are private, local (short range), but where competing cable systems run at very high speeds. WiFi achieves greater than 10MBit/ Sec throughput for a user in many circumstances. Currently WiFi carries more user data than any other wireless technology. Evolution is to go further, faster and at lower power consumption [2]

Upstart wireless LAN [WLAN] technologies under the 802.11 (Wi-Fi) umbrella have leapfrogged towards cellular and other efforts edging towards broadband wireless [ such as 802.16 / WiMAX ] and have led to the first wide spread , commercially successful broadband wireless access technology . Infact, Wi-Fi is a runaway success around the globe [5]

4. Proposed Block Diagram of Transmitter

As discussed earlier, the transmitter block is divided in to five parts as shown in fig 4 and only two blocks are considered for VHDL simulation. These are Payload Data Storage block & Data Processing block.

4.1 Payload Data storage block:

Is further divided into two modules i.e. FIFO module & Data length counter module. These modules are discussed as shown below.

4.1a. FIFO Module

Description:

FIFO Module is shown in Figure 4.1 a. It contains the data to be transmitted. It acts as the synchronizing tool i.e. the data are entered at high rate but it is retrieved at the slower rate. Here, we have taken 32x8 bits of data storage. Here, the first incoming data goes out first.

It acts on two clocks i.e. SysClk and ByteClk, on their rising edge and when the FIFO is enabled the input data is retrieved. The Full and Empty signals shows the state of the FIFO.
There are two types of widely used hardware module: Serializer, HEC and CRC and they are discussed in details as shown below.

### 4.2a. Serializer Module:

**Description:**

Fig. 4.2 a shows Serializer Module. It is basically the parallel input and serial output device. Various data selected at the multiplexer are serially obtained. It occurs at every rising edge of the clock and when the serial enable is high. The output bit is designated as SBit. When all the output bits are over, then the End of Conversion i.e. EOC goes high.

### 4.2b. HEC Module:

**Description:**

Fig. 4.2 b shows HEC Module. This module produces the Head Error Check bits. It is the 16-bit error check bit. The HEC is calculated when the HRCCalEna is high and when the TxEHa is high then the HEC data is transmitted along with the PLCP Header Bits.

### 4.2c. CRC Module:

**Description:**

Fig. 4.2 c shows CRC Module. The CRC is 32 bit field containing the 32-bit Cyclic Redundancy Check. When the TxEHa signal is high, then the CRC data is given out and when the CRCCalEna is high, then the CRC is calculated. CRCOver is high when the transmission of the data is over. This module helps in error free transmission of the data with proper reliability.

5. **VHDL Modeling of Wi-Fi MAC layer for Transmitter:**

There are two types of widely used hardware description languages i.e. Verilog HDL with C-language like syntax, easy to learn and another is VHDL which follows the structure of ADA programming language. Verilog and VHDL each have about 50% share of the commercial user base [8].

VHDL is an acronym for VHIC i.e. very large scale integrated circuit hardware description language. It was standardized by IEEE. VHDL is used for synthesis construct and implement a design on silicon. VHDL is used for simulation to imitate real world scenarios for verification [9].

Due to high computational complexity of WLAN systems and the capabilities of state-of-the-art microprocessors, an implementation based solely on microprocessors would require a large number of components and would be cost inefficient for FPGAs with their spatial/parallel computation style can significantly accelerate complex parts of WLANs and improve the efficiency of discrete components implementations [10].

The design has been synthesized using FPGA. This device belongs to the Virtex-II group of FPGAs from Xilinx. Two types of FPGAs (Field Programmable Logic Array) are available i.e. i) Reprogrammable (SRAM-based) from Xilinx, Altera, Lattice and Atmel ii) One-time Programmable (OTP) from Actel, Quick logic.

FPGAs are reasonably cheap, with short design cycle and are reprogrammable. They are more flexible than PLDs and more compact than MSI/SSLS. FPGAs have evolved to meet new application demands with features like i) Newer devices incorporate entire CPUs i.e. Xilinx Virtex II pro has 1-4 power PC CPUs ii) Have carry chains to have a better support for multi-bit operations iii) Have integrated memories, such as block RAMs in the devices we use iv) Have specialized units, such as Multipliers to implement functions that are Slow/inefficient in CLBs [Configurable Logic Blocks] [6].

FPGA enables high performance due to the following factors i) Tailoring to desired bit-width (ii) Ease of applying varying sample rates (iii) Flexibility of parallel execution of basic functions due to uniform architectural
resources [7] Here, two modules of Wi-Fi MAC layer transmitter are chosen and implemented on an FPGA device. The details of simulation are shown in Table 1.

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<th>Value</th>
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6. Simulation results & discussion:

The payload data storage and data processing blocks consist of a total of five different individual modules i.e. FIFO, Data length counter modules and serializer, HEC, CRC modules respectively all these modules are simulated using modelsim and simulation results are shown in Fig 6.1a, 6.1b, 6.1c, 6.1d and 6.1e.

6.1. a Simulation results of FIFO Module:

Fig 6.1a Simulation indicates enabling of FIFO on the raising edge of two clocks SysClk and ByteClk.

6.1.b Simulation results of Data length counter:

Fig 6.1b Simulation indicates that when the number of data is equal to the maximum number, then a Data Cnt Over signal goes high.

6.1.c Simulation waveforms serializer module:

Fig 6.1c Simulation indicates the end of output bits, EOC goes high.

6.1.d Simulation results of HEC module:

Fig 6.1d Simulation indicates that when the T*Ena is high, HEC Data is transmitted along with PLCP Header bits.

6.1.e Simulation results of CRC module:

Fig 6.1e Simulation indicates, at the end of transmission of data, CRC Over goes high.
7. Conclusions:

Various individual modules of Wi-Fi Transmitter have been designed, verified functionally using VHDL – simulator, synthesized by the synthesis tool. This design of the Wi-Fi transmitter is capable of transmitting the frame formats. The formats include all 802.11 frames i.e. MAC frame, RTS frame, CTS frame and ACK frame. The transmitter is also capable of generating error-checking codes like HEC and CRC. It can handle variable data transfer.

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References:

2) Broadband wireless Access, Institution of Engineering and Technology Seminar, 6th Dec 2006, London, UK
4) Shambhu Upadhyaya, “Wireless Network Security,” Lecture 5, University at Buffalo, the State University of Newyork
7) Introduction to DSP Design flow, 2006 Xilinx, Inc
8) Janak. H.Patel, Introduction to VHDL 1 and 2, Dept of Electrical and Computer Engineering, University of Illinois at urbana- campaign.